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SUGHRUE, MION, ZINN, MACPEAK & SEAS
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EXAMINER

THANGAVELU, KANDASAMY

ART UNIT	PAPER NUMBER
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2123

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS / from the mailing date of this communication.

Office Action Summary

Application No.

09/273,560

Applicant(s)

HASEGAWA, TAKUMI

Examiner

Kandasamy Thangavelu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 November 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 March 1999 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' Amendment mailed on November 16, 2006. Claims 1-4 of the application were amended. Claims 1-4 of the application are pending. This office action is made final.

Claim Objections

2. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

3. Claims 3 and 4 are objected to because of the following informalities:

Claim 3, Line 10, "said output terminals" appears to be incorrect and it appears that it should be "each output terminal" since there is only reference to each output terminal previously.

Claims 3, Line 12, "the delay time" appears to be incorrect and it appears that it should be "delay time" since there is reference to only delay time information previously.

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Claim 4, Line 12, "said output terminals" appears to be incorrect and it appears that it should be "each output terminal" since there is only reference to each output terminal previously.

Claims 4, Line 12, "the delay time" appears to be incorrect and it appears that it should be "delay time" since there is reference to only delay time information previously.

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. §112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 3-4 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

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5.1 Amended claim 3, Lines 3-5 state, “said delay analysis library comprising connection information, delay time information and **logic operation delay information**”.

The specification does not describe anywhere the **logical operation delay information**. The specification only describes the **logical operation information** and **delay information** for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information.

The **logical operation delay information** is *new material* introduced in the amendment of March 31, 2006 and not found in the original specification and therefore this amendment is not allowed.

5.2 Amended claim 4, Lines 5-7 state, “said delay analysis library comprising connection information, delay time information and **logic operation delay information**”.

The specification does not describe anywhere the **logical operation delay information**. The specification only describes the **logical operation information** and **delay information** for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information.

The **logical operation delay information** is *new material* introduced in the amendment of March 31, 2006 and not found in the original specification and therefore this amendment is not allowed.

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6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites at Lines 9 and 11, "said at least one circuit". There is insufficient antecedent basis for "said at least one circuit" in the claim.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

9. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Blinne et al.** (U.S. Patent 5,274,568) in view of **Hasegawa** (U.S. Patent 6,041,168) and further in view of **Hasegawa** (U.S. Patent 5,528,511).

10.1 **Blinne et al.** teaches method of estimating logic cell delay time. Specifically, as per Claim 1, **Blinne et al.** teaches the delay analysis system for making a delay analysis of a logic circuit (Col 1, Lines 7-13);

the system having a delay analysis library (Col 1, Lines 9-13); and
comprising connection information and delay time information for a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

Blinne et al. does not expressly teach that for at least one circuit of the plurality of circuits, the library further comprises logical operation information. **Hasegawa** '168 teaches that for at least one circuit of the plurality of circuits, the library further comprises logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Blinne et al.** with the system of **Hasegawa** '168 that included for at least one circuit of the plurality of circuits, the library further comprising logical operation information, because delay verification time could be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35).

Blinne et al. and **Hasegawa** '168 do not expressly teach that delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and

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wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, and wherein the delay time information for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information. **Hasegawa '511** teaches that delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, and wherein the delay time information for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified). It would have been obvious to one of ordinary skill in the art at the time of

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Applicant's invention to modify the system of **Blinne et al.** and **Hasegawa** '168 with the system of **Hasegawa** '511 that included delay time information provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information was specific to an input terminal logical state transition and resulting logical state transition at an output terminal, and wherein the delay time information for each signal path of the logical circuit of the at least one circuit was based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information, because this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process (Col 2, Lines 61-65).

10.2 As per Claim 2, **Blinne et al.** teaches the delay analysis system for making a delay analysis of a logic circuit (Col 1, Lines 7-13);

the system having a delay analysis library (Col 1, Lines 9-13); and

comprising connection information and delay time information for a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

Blinne et al. does not expressly teach that for each of the plurality of circuits, the library further comprises logical operation information. **Hasegawa** '168 teaches that for each of the plurality of circuits, the library further comprises logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35).

Blinne et al. and **Hasegawa** '168 do not expressly teach that delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and wherein a delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal for each circuit of the plurality of circuits,

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and wherein the delay time information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information for the at least one circuit.

Hasegawa '511 teaches that delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and wherein a delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal for each circuit of the plurality of circuits, and wherein the delay time information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information for the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

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10.3 As per Claim 3, **Blinne et al.** teaches a method for making a delay analysis of a logic circuit (Col 1, Lines 7-13); comprising the steps of:

referencing a delay analysis library for a plurality of circuits (Col 1, Lines 9-13);

the delay analysis library comprising connection information, and delay time information (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

Blinne et al. does not expressly teach the delay analysis library comprising logic operation delay information. **Hasegawa '168** teaches library comprising logic operation delay information (Col 1, Lines 58-61 and Col 2, Lines 31-35).

Blinne et al. and **Hasegawa '168** do not expressly teach that delay time information is provided for a signal path from input terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of the plurality of circuits, the delay time information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by logical operation information for the at least one circuit. **Hasegawa '511** teaches that delay time information is provided for a signal path from input terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of the plurality of circuits, the delay time information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by logical operation information for the at least one circuit (Fig.

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3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

Blinne et al. and **Hasegawa '168** do not expressly teach if the logic circuit comprises the at least one circuit, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information.

Hasegawa '511 teaches if the logic circuit comprises the at least one circuit, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the

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input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information (CL1, L28-35; Col 2, Lines 30-42; Col 3, Lines 5-26).

10.4 As per Claim 4, **Blinne et al.** teaches a computer-readable medium having stored thereon a program comprising computer instructions that, when executed on a computer perform a process for executing a delay analysis method for a logic circuit, the computer readable medium causing a computer to execute the method (Col 2, Lines 42-50); wherein the method comprises:

- referencing a delay analysis library for a plurality of circuits (Col 1, Lines 9-13);
- the delay analysis library comprising connection information and delay time information (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

Blinne et al. does not expressly teach the delay analysis library comprising logic operation delay information. **Hasegawa '168** teaches that the library comprising logical operation delay information (Col 1, Lines 58-61 and Col 2, Lines 31-35).

Blinne et al. and **Hasegawa '168** do not expressly that delay time information is provided for a signal path from input terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of the plurality of circuits, the delay time information for each signal path of the at least one circuit is based upon logical state transitions

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at the input terminals and corresponding logical state transitions at the output terminals as represented by logical operation information for the at least one circuit. **Hasegawa '511** teaches that delay time information is provided for a signal path from input terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of the plurality of circuits, the delay time information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by logical operation information for the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

Blinne et al. and Hasegawa '168 do not expressly teach if the logic circuit comprises the at least one circuit, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high

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state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information.

Hasegawa '511 teaches if the logic circuit comprises the at least one circuit, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information (CL1, L28-35; Col 2, Lines 30-42; Col 3, Lines 5-26).

Blinne et al. and Hasegawa '168 do not expressly teach performing a delay calculation to determine a propagation delay time using the selected delay time of the at least one circuit.

Hasegawa '511 teaches performing a delay calculation to determine a propagation delay time using the selected delay time of the at least one circuit (Col 3, Lines 5-26).

Response to Amendments

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11. Applicants' amendments, filed on November 16, 2006 have been considered.

Applicant's arguments with respect to claim rejections under 35 USC 103 (a) are not persuasive.

11.1 As per the applicants' argument that "Hasegawa '511 fails to teach a delay time information that is specific to an input terminal logical state transition and resulting logical state transition at an output terminal as taught by the subject application; Blinne et al., Hasegawa '168 and Hasegawa '511 fail to teach or suggest, either alone or in combination, a delay time information that is specific to an input terminal logical state transition and resulting logical state transition at an output terminal"; the examiner respectfully disagrees.

Hasegawa '511 shows at Fig. 3 the logical state transitions at each input terminal and logical state transitions at each output terminal. **Hasegawa '511** discusses at Col 1, Lines 28-35 the logical state transitions at the input terminal and the output terminal, using rise/fall terms. **Hasegawa '511** states at Col 2, Lines 30-42 that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid). The logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit. **Hasegawa '511** describes at Col 3, Lines 5-26 that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified. Therefore, **Hasegawa '511** teaches a delay time information that is specific to an input terminal logical state transition and resulting logical state

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transition at an output terminal, as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65).

11.2 As per the applicants' argument that "Hasegawa '511 teaches a delay time verifying, wherein the rise and fall are not permitted between nodes connected by a short circuit (Col 3, L3-26); Hasegawa '511 confusingly teaches an OR gate which fails to respond to two simultaneously hi inputs (Fig.3); Hasegawa '511 teaches that input and output paths in a given OR gate are equal with respect to delay; ... the Examiner appears to acknowledge the overall arguments; however, the Examiner repeats arguments from the main body of the Office Action rather than specifically addressing Applicant's analysis as to why Hasegawa '511 is deficient; the Examiner is requested to specifically address the Applicant's analysis of Hasegawa '511", the examiner respectfully disagrees.

The examiner takes the position that Hasegawa '511 does not teach at Col 3, L3-26, a delay time verifying, wherein the rise and fall are not permitted between nodes connected by a short circuit; Hasegawa '511 does not confusingly or otherwise teach at Fig.3, an OR gate which fails to respond to two simultaneously hi inputs. Hasegawa '511 does not teach that input and output paths in a given OR gate are equal with respect to delay. The Examiner does not appear to acknowledge the arguments of the applicant since they are all are not there in Hasegawa '511. The applicant's analysis as to why Hasegawa '511 is deficient is incorrect and the examiner does not agree with the applicant's analysis.

Conclusion

ACTION IS FINAL

12. Applicant's arguments with respect to claim rejections under 35 USC § 103 (a) are not persuasive. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

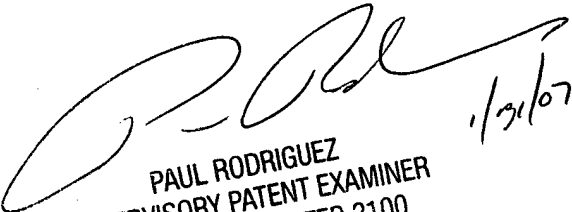
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
January 20, 2007


PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
1/21/07